IN THE CLAIMS

1. (currently amended) A method of making a microelectronic package, comprising:

providing a dielectric layer having a top side and a bottom side;

forming a top conductive feature on the top side of the dielectric layer and forming a bottom conductive feature on the bottom side of the dielectric layer~~;~~, said top and bottom conductive features being solder-wettable;

juxtaposing the dielectric layer with at least one microelectronic element having contacts and bonding the contacts of the microelectronic element with the bottom conductive feature;

forming a via through the dielectric layer either before or after said bonding step, the via being aligned with the top conductive feature and the bottom conductive feature; and

electrically interconnecting the top conductive feature and the bottom conductive feature through the vias by depositing electrically-conductive material in the vias without seeding the vias, said electrically-conductive material being a blob or solder which adheres to said top and bottom conductive features.

2. (cancelled).

3. (currently amended) A method of forming a microelectronic package, comprising:

a) providing a dielectric layer with a top side, a bottom side, a top metal layer on the top side, and a

bottom metal layer on the bottom side;

b) forming first apertures in the top metal layer and forming vias in the dielectric layer aligned with the first apertures;

c) applying a first resist to the top metal layer, applying a second resist to the bottom metal layer and patterning the first resist and second resist in the same step to form first openings in the first resist and second openings in the second resist;

d) the first openings leaving uncovered portions of the top metal layer surrounding the vias, and the second openings being aligned with the first openings;

e) forming top conductive features from portions of the top metal layer aligned with the first openings and bottom conductive features on portions of the bottom metal layer aligned with said second openings;

f) juxtaposing the dielectric layer with a microelectronic element so that the bottom conductive features are aligned with contacts of the microelectronic element; and

g) electrically interconnecting the top conductive features and the bottom conductive features through the vias by depositing electrically conductive material in the vias without seeding the vias~~.~~, wherein the bottom conductive features include pads at an end of the bottom conductive features and the method includes bonding the pads to the contacts of the microelectronic element.

4. (original) The method of claim 3, further comprising bonding the bottom conductive features to the contacts of the microelectronic element.

5. (cancelled) The method of claim 3, wherein the

bottom conductive features include pads at an end of the bottom conductive features and the method includes bonding the pads to the contacts of the microelectronic element.

6. (currently amended) A method of forming a microelectronic package, comprising:

a) providing a dielectric layer with a top side, a bottom side, a top metal layer on the top side, and a bottom metal layer on the bottom side;

b) forming first apertures in the top metal layer and forming vias in the dielectric layer aligned with the first apertures;

c) applying a first resist to the top metal layer, applying a second resist to the bottom metal layer and patterning the first resist and second resist in the same step to form first openings in the first resist and second openings in the second resist;

d) the first openings leaving uncovered portions of the top metal layer surrounding the vias, and the second openings being aligned with the first openings;

e) forming top conductive features from portions of the top metal layer aligned with the first openings and bottom conductive features on portions of the bottom metal layer aligned with said second openings;

f) juxtaposing the dielectric layer with a microelectronic element so that the bottom conductive features are aligned with contacts of the microelectronic element;

g) electrically interconnecting the top conductive features and the bottom conductive features through the vias by depositing electrically conductive material in the vias without seeding the vias;

h) bonding the bottom conductive features to

the contacts on the microelectronic element; and

i) moving the microelectronic element and the dielectric layer with respect to one another after the step of bonding so that the bottom conductive features are deformed into a vertically extensive shape.

7. (original) The method of claim 6, wherein the step of electrically interconnecting is performed after the step of moving.

8. (withdrawn) A method of making a microelectronic package, comprising:

a) providing a dielectric layer with a top side, a bottom side, a top metal layer on the top side, and a bottom metal layer on the bottom side;

b) forming first apertures in the top metal layer and top conductive features surrounding the first apertures, the top conductive features being formed from portions of the top metal layer;

c) forming bottom conductive features at portions of the bottom metal layer;

d) the bottom conductive features being aligned with the first apertures;

e) juxtaposing a microelectronic element with the dielectric layer so that the bottom conductive features are aligned with contacts of the microelectronic element;

f) forming vias in the dielectric layer, either before or after the step of juxtaposing, the vias being aligned with the first apertures; and

g) electrically interconnecting the top conductive features and the bottom conductive features through the vias by depositing electrically conductive material in the

vias without seeding the vias, the electrically interconnecting being performed either before or after the step of juxtaposing.

9. (withdrawn) The method of claim 8, further comprising bonding the bottom conductive features to the contact of the microelectronic element.

10. (withdrawn) The method of claim 9, wherein the bottom conductive features include pads at an end of the bottom conductive features and the method includes bonding the pads to the contacts of the microelectronic element.

11. (withdrawn) The method of claim 9, further comprising moving the microelectronic element and the dielectric layer with respect to one another after the step of bonding so that the bottom conductive features are deformed into a vertically extensive shape.

12. (withdrawn) The method of claim 11, wherein the step of electrically interconnecting is performed after the step of moving.